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7E1827

B.Tech. VII-Sem. (Main) Examination, December - 2023
Electronics & Comm. Engg.
7EC5-11 VLSI Design

Time : 3 Hours **Maximum Marks : 70**

Instructions to Candidates:

Attempt all Ten questions from Part A, five questions out of seven questions from Part B and three questions out of five questions from Part C.

(Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205).

PART - A

(Answer should be given up to 25 words only)

All questions are compulsory. **(10×2=20)**

1. List the basic process of IC fabrication.
2. What is body effect? Explain it.
3. Define short channel devices.
4. What are the different operating regions for an MOS transistor?
5. Give the various color codings used in stick diagram.
6. What is meant by transmission gate?
7. What is a task in verilog. Mention few data types in Verilog.
8. How do you prevent latch-up problems?
9. Write any five advantages of CMOS process?
10. Explain the process of channel length modulation.

PART-B

Analytical/Problem Solving questions. Attempt any Five questions. (5×4=20)

1. Derive the CMOS inverter dc characteristics and obtain the relationship for output voltage at different region in the transfer characteristics.
2. Differentiate between scaling and biasing. Also draw the MOS transistor circuit model.
3. Describe the operation of NMOS enhancement transistor Also explain the process of semiconductor fabrication.
4. Define the concept involved in timing control in VERILOG. list the types of ports in verity.
5. State & drive the analysis of speed and power dissipation of CMOS Invecter.
6. Differentiate between clocked CMOS logic and DOMINO logic and NORA logic with the required example.
7. Describe the word combinational logic. Explain
   a) Registers
   b) Compound gates
   c) Multiplexes.
   d) Basic gates

PART - C

(Descriptive/Analytical/Problem Solving/Design questions).

Attempt Any Three Questions. (3×10=30)

1. What are the different factors affecting the threshold voltage of MOSFET? Drive the formula used. Also derive the body effect coefficient.
2. Describe the process of layout optimization using Eular path. What do you mean by DRc rules for layout. Also explain the latch-up problem.
3. Define basic memory circuits. Explain SRAM and DRAM in detail. Derive the pull up to pull down ratio ($\beta p/\beta n$).
4. Write the VHDL code for Positive edge triggered S-R flip flop. Also with VHDL code for half adder in structural style.
5. Compare NORA and NP (ZIPPER) CMOS logic structures. Also explain the following:-
   i) Shift Registers.
   ii) Flip-flops.

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7E1727

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7E1727

B.Tech. VII-Sem. (Back) Examination, December - 2023
Electronics and Communication Engineering
7EC5-11 VLSI Design

Time : 3 Hours **Maximum Marks : 120**
Min. Passing Marks : 42

Instructions to Candidates:

*Attempt All **Ten** questions from Part A, **Five** questions out of **Seven** from Part B and **Four** questions out of **Five** from Part C.*

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205).

PART - A

(Answer should be given up to 25 words only)

All questions are Compulsory. **(10×2=20)**

1. Why NMOS technology is preferred more than PMOS technology
2. What are the process involved in Photo lithography?
3. List the advantages and disadvantages of SOI process.
4. Distinguish electrically alterable and non electrically alterable ROM.
5. Write down the basic steps of IC fabrication.
6. What is pull down device?
7. Describe the Channel - length Modulation.
8. Give the various Color coding used in stick diagram.
9. Compare between CMOS and bipolar technologies.
10. What are the Commonly used Conducting layers used in IC fabrication.

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PART-B

(Analytical/Problem Solving questions)

Attempt any Five questions. **(5×8=40)**

1. What do you mean by Power dissipation?
   Define pull up to pull down ratio (B_p/B_n)

2. Write the design style.classification?
   What are the two types of ASIC's?

3. Describe various circuit techniques used in domino CMOS circuit for solving change sharing problem.
4. Write VHDL code for half adder in a structural style.
5. Design the following logic circuits using CMOS logic gate:
   i) 3 - input nand gate
   ii) S-R Flip - Flop
6. Define shift registers. Explain the following terms in detail
   i) NP logic
   ii) PE logic
   iii) NORA logic
7. What is latch-up problem in CMOS? Draw and explain its physical origin model and V-I characteristics.

PART - C

(Descriptive/Analytical/Problem Solving/ Design questions) **(4×15=60)**

Attempt Any Four Questions.

1. What is the need for testing. List any two facts that occur during manufacturing?
2. Describe the steps in ASIC design flow. Write down the characteristics of FPGA. Also explain programmable logic array.
3. Write short note on the following:
   a) Flip - flop
   b) Logic Gates
   c) Hot electron Object
   d) Power dissipation.
4. Differentiate between narrow channel effect and punch through effect. Also define the compound gates in detail
5. Describe optimization using Eular path. list out the DRC Rules for layout and issues of interconnect.

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7E1729

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7E1729

B.Tech. VII-Sem. (Back) Examination, December - 2023
Electronics and Communication Engineering
7EC5-13 CMOS Design

Time : 3 Hours **Maximum Marks : 120**
Min. Passing Marks : 42

Instructions to Candidates:

Attempt All Ten questions from Part A, Five question out of Seven from Part B and Four questions out of Five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205).

PART - A

(Answer should be given up to 25 words only)

All questions are Compulsory. **(10×2=20)**

1. What is Noise Margin?
2. Explain sizing of the inverter.
3. Why is NAND gate preferred over NOR gate for fabrication?
4. What is latch up?
5. What is Body Effect?
6. What is the fundamental difference between a MOSFET and BJT?
7. Which transistor has higher gain. BJT or MOS and why?
8. Difference between SRAM and DRAM.
9. Mention different clock mechanisms.
10. Draw a 1 - Transistor dynamic RAM cell

PART-B

(Analytical/Problem Solving questions)

Attempt any Five questions. **(5×8=40)**

1. What is the threshold Voltage of MoS device and its significance?
2. What is 'Euler Path'? What is its use?Explain with suitable example.
3. Derive the propagation delay of NMOS inverter.
4. What is a stick diagram and explain different symbols and components in stick diagram?
5. Explain NORA CMOS logic circuit in detail.
6. What is C^2 MOS logic? Draw any logic circuit wing it.
7. Derive the propagation delay of NHOS inverter.

PART - C

(Descriptive/Analytical/Problem Solving/ Design questions)

Attempt Any Four Questions. **(4×15=60)**

1. Write the layout design rules and draw diagram of 4 i/P NAN and NOR gate.
2. Explain the building block architecture of FPGA.
3. What do you mean by VHDL ? Write the VHDL code for
   a) Full adder
   b) D flip-flop
4. Draw the following circuits
   i) $y = A\,\overline{B}\,C$ using CMOS
   ii) 1 bit memory cell using CMOS
   iii) $y = A \oplus B$ using transmission gate.
5. Explain the dynamic behaviour of MOSFET transistor with neat diagram.

7E7081

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7E7081

B.Tech. VII-Sem. (Back) Examination, December - 2023
Electronics & Communication Engg.
7EC1A Antenna & Wave Propagation

Time : 3 Hours **Maximum Marks : 80**
Min Passing Marks: 24

Instructions to Candidates:

Attempt any **five questions,** selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

UNIT -I

1. With the help of neat diagrams explain the principle of radiation mechanism in antennas, also derive the relationship between effective aperture area and gain of antenna **(16)**

(OR)

1. a) Draw the equivalent circuit of an antenna, also Prove the reciprocity theorem.

   b) Define beamwidth and beam solid angle. **(8+8)**

UNIT -II

2. Explain the effects of uniform and non-uniform amplitude distributions in array? Also explain how to select current excitations in an array to avoid side lobes in radiation pattern? **(16)**

(OR)

2. An array contains 100 isotropic radiators with an inter element spacing of 0.5λ. It is required to produce broadside and end-fire beams. Find Null-to-Null beam width and half-power beam width in degrees. **(16)**

UNIT -III

3. Derive the expression for pitch angle to get circularly polarized radiation pattern for a helical antenna, operating in broadside mode and sketch its pattern. **(16)**

(OR)

3. Explain the need and configuration of a folded dipole antenna. Sketch its radiation pattern and compare its characteristics with those of a simple half wave dipole. **(16)**

UNIT -IV

4. a) Describe briefly the salient features of ground wave propagation

   b) Write short notes on duct propagation . **(8+8)**

(OR)

4. a) What should be the polarization of EM wave for the ground wave propagation? Justify.

   b) Write short notes on Tropospheric scattering. **(8+8)**

UNIT -V

5. a) Derive the relationship between MUF and critical frequency.

   b) What three main factors determine the amount of refraction in the ionosphere? **(8+8)**

(OR)

5. a) Discuss experimental determination of virtual heights and critical frequencies.

   b) What is the density of free electrons in the ionospheric layer at critical frequency of 1.3 MHz? **(8+8)**

7E7072

Roll No. _____ [Total No. of Pages : 2

7E7072

B.Tech. VII-Sem. (Back) Examination, December - 2023
Electronic Instrumentation & Control Engg.
7EI2A Digital Signal Processing

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 24

Instructions to Candidates:

*Attempt any **Five** questions, selecting **One** question from **each unit**. All questions carry **Equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Use of following supporting material is permitted during examination. (Mentioned in form No. 205).

UNIT - I

1. a) State Shannon's Sampling theorem. Explain sampling with zero order hold and reconstruction of singals. (8)

   b) Define Aliasing with suitable waveform. Explain its effect and how it can be prevented. (8)

(OR)

1. a) Draw the block diagram of continuous time processing of discrete time signals and write mathematical expression in terms of time domain and frequency domain for output of each stage. (8)

   b) Determine the nyquist rate and nyquist interval for the following signal $x(t)=\frac{1}{\pi t}\sin(500\pi t)$. (8)

UNIT - II

2. a) Define minimum phase system, write-.
   i) Generalized expression of minimum phase (4)
   ii) Discuss stability and causality condition for a discrete system. (4)

   b) Write short note on:
   i) All pass systems (4)
   ii) LCCD (4)

(OR)

2. a) Determine the homogeneous solution of the system $y(n)-3y(n-1)-4y(n-2)=x(n)$. **(8)**

   b) Check whether the following system are linear- **(8)**

   i) $F[x(n)]=an\ x(x)+b$

   ii) $F[x(n)]=e^{x(n)}$

UNIT - III

3. a) Explain cascade and parallel realization of IIR systems with example. **(8)**

   b) Explain the FIR system and transposed form. **(8)**

(OR)

3. a) Draw the block and singal flow graph representation of LCCD equations. **(16)**

UNIT - IV

4. Write short note on following:

   i) Bilinear Transformation. **(8)**

   ii) Impulse invariance Transformation. **(8)**

(OR)

4. a) Describe Chebyshev filters with its response. **(8)**

   b) Discuss FIR filters by windowing technique. Give the filter response of all window functions. **(8)**

UNIT - V

5. a) Explain the properties of Discrete Fourier Transform (DFT). **(8)**

   b) Explin DIT (Decimation-In-Time) algorithm. **(8)**

(OR)

5. Determine the four point DFT of the sequence $x(n)=(1,0,2,1)$ using DIT algorithm. **(16)**
